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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,438	08/27/2003	Hideki Morii	12480-000020/US	4537

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EXAMINER	
SHENG, TOM V	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 09/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,438	MORII, HIDEKI	
	Examiner	Art Unit	
	Tom V. Sheng	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *4-8 and 10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,11 and 12* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/27/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Species 1 in the reply filed on 6/27/2006 is acknowledged. The traversal is on the ground(s) that the search required for each of Species 1-6 would not place an undue or serious burden on the Examiner. This is not found persuasive because even though some of the Species might involves similar class/subclasses, the features to search are still different and involves careful considerations. Moreover, claim 10 involves layout of row drive circuit including a dummy row line and the search involved would not be similar to Species 1 at all.

The requirement is still deemed proper and is therefore made FINAL.

Drawings

2. Figures 18-31 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 1 and 9 are objected to because of the following informalities:

As for claim 1, line 24, please insert --wherein -- before "during", line 27, please replace "generating" with --first generates--, and line 31, please replace "supplying" with --supplies--.

As for claim 9, line 37, please replace "a" with "the".

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

4. Claims 1-3 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claim 1, lines 31-32 and claim 11, lines 32-33, it is unclear as to the scope of "then supplies the row drive timing signal, which has been generated, to the row drive circuit." Particularly, the Examiner is concerned with which output terminals, if any, of the row drive circuit would then be driven and whether the first output terminal would be driven again with the row drive signals. Claims 2-3 are dependent on claim 1.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art, hereinafter APA, in view of Park et al. (US 2002/0033787 A1), hereinafter Park.

As for claim 1 and associated claims 11 and 12, APA teaches a display device, comprising:

a display panel (LCD device 101; fig. 18) on which pixels corresponding to respective intersections of row lines and column lines are provided in a matrix manner (pixel PIX is provided at each intersection between the gate lines G and the source lines S; page 2, lines 9-11);

a row drive circuit (gate driver 102; fig. 18 and 23; page 2, lines 1-4) which receives a row drive timing signal (fig. 27e; gate clock signal GCK and gate start pulse GSP) for driving the row lines of the display panel (fig. 27f), and sequentially supplies row drive signals for driving the row lines to the respective row lines connected to the pixels, in accordance with the row drive timing signal (fig. 24; gate signals for respective terminals OG1-OG768 to corresponding gate lines G1-G768 are serially provided; page 9, lines 1-8; also page 11, line 17 through page 12, line 2);

a column drive circuit (source driver 103) which receives display data and a column drive timing signal (source start pulse signal SSP and latch strobe signal LS) for driving the column lines of the display panel (fig. 27c; for shifting and latching each line of data DH1, ..., DH768; page 11, lines 4-14), and supplies column drive signals (source signals) corresponding to the display data (correspond to each of DH1, ...,

DH768) to the respective column lines connected to the pixels (i.e. D1 to column 1, etc.), in accordance with the column drive timing signal (analyzed above); and

a control device (timing control ASIC 108; fig. 28) which receives the display data (Input Data), a data enable signal (ENAB), and a clock signal (CK),

generates the row drive timing signal (gate clock signal GCK, gate start pulse signal GSP) from the data enable signal and the clock signal (page 13, line 9 through page 14, line 2) and outputs the row drive timing signal to the row drive circuit (inherent), and

generates the column drive timing signal (latch strobe signal LS, source clock signal SCK and the source start pulse signal SSP) from the data enable signal and the clock signal (page 13, line 9 through page 14, line 2) and supplies the column drive timing signal to the column drive circuit (inherent), along with the display data (as buffered output data; page 14, lines 6-9).

As analyzed above, the timing control ASIC 108 generates the row drive timing signal such that gate signals to output terminals OG1-OG768 are sequentially provided. However, the APA admits failure to drive the dummy gate line connected to the first output terminal OG0. Thus, APA does not teach "wherein during a period from the timing of inputting the data enable signal to a start of outputting the column drive signals of a first horizontal period of one vertical period, the control device first generates the row drive timing signal with reference to a timing of inputting the data enable signal in order to cause one of the row drive signals to be supplied to a first output terminal of the

row drive circuit, and then supplies the row drive timing signal, which has been generated, to the row drive circuit."

Park teaches a liquid crystal display with a dummy first gate line such that all the storage capacitors of the pixels have the same charging characteristics to ensure a uniform brightness in display (dummy gate line 116; fig. 4; page 3, paragraphs 39 and 40). Specifically, Park teaches that, it is preferable to provide a dummy gate signal preceding the first gate signal on gate line G1 (page 3, paragraph 43). Park further teaches a dummy gate signal producing circuit 200 that receives a vertical synchronizing signal (VS) and a data enable signal (DE) to produce the dummy gate signal preceding the first gate signal. See fig. 6 and 7 and page 3, paragraphs 46. Note that the pulse signal A would be level shifted to the level of a gate signal.

One of ordinary skill in the art would recognize that, since Park's dummy gate signal generation is based on a data enable signal, Park's dummy gate signal producing circuit 200 could be incorporated in APA's timing control ASIC 108. With this, the problem with driving the dummy gate line via the first terminal OG0 is resolved and uniform brightness in display is ensured.

Allowable Subject Matter

7. Claim 9 is objected due to a minor error and would be allowed upon correction.

8. The following is a statement of reasons for the indication of allowable subject matter: none of the prior arts of record teaches the limitations, "a shift clock signal generation section which generates a first clock of a shift clock signal which determines

a timing to shift the start pulse signal, when a predetermined number of clocks of the clock signal is counted from the timing of inputting the data enable signal, the row drive circuit obtaining the start pulse signal in accordance with the first clock of the shift clock signal, so as to cause one of the row drive signals to be outputted to a first output terminal" of claim 9.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lim (US Patent No. 6,812,908) teaches a liquid crystal display with a dummy gate line (fig. 4 and 5). Driving of the dummy gate line is synchronized with the time at which the mth or last gate line is being driven. That is, the driving of the dummy gate line is part of the horizontal scanning of gate lines during display operation. Moreover, Lim does not teach of a control device that receives display data, a data enable signal and a clock signal and generates in response row drive timing signal to the row drive circuit (i.e. gate driver IC) and data drive timing signal and display data to the column drive circuit (i.e. data driver IC). Lim also does not teach generating a first clock of a shift clock signal which determines a timing to shift the start pulse signal, when a predetermined number of clocks of the clock signal is counted from the timing of inputting the data enable signal, or obtaining the start pulse signal in accordance with a first clock of the shift clock signal, so as to cause one of the row drive signals to be outputted to a first output terminal.

Nishikubo et al. (US Pub. No. 2001/0050678) teaches a gate driver IC for the scanning of gate lines for display. Specifically, each gate driver IC A (fig. 2 and 3) has at least one output terminal (such as OG1) for driving a dummy gate line. The gate clock GCK and gate start pulse GSP are from a timing control IC. The GSP is supplied to shift register R2 instead of R1 and output from R257 is fed to R1. As a result of the sequential scanning, OG1 (for driving a dummy gate line G0) and OG258 (for driving the GSP for the next cascade connected gate driver IC) are supplied in parallel. Nishikubo et al. does not teach generating a first clock of a shift clock signal which determines a timing to shift the start pulse signal, when a predetermined number of clocks of the clock signal is counted from the timing of inputting the data enable signal, or obtaining the start pulse signal in accordance with a first clock of the shift clock signal, so as to cause one of the row drive signals to be outputted to a first output terminal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tom V. Sheng whose telephone number is (571) 272-7684. The examiner can normally be reached on 9:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tom Sheng
September 9, 2006

AMR A. AWAD
SUPERVISORY PATENT EXAMINER